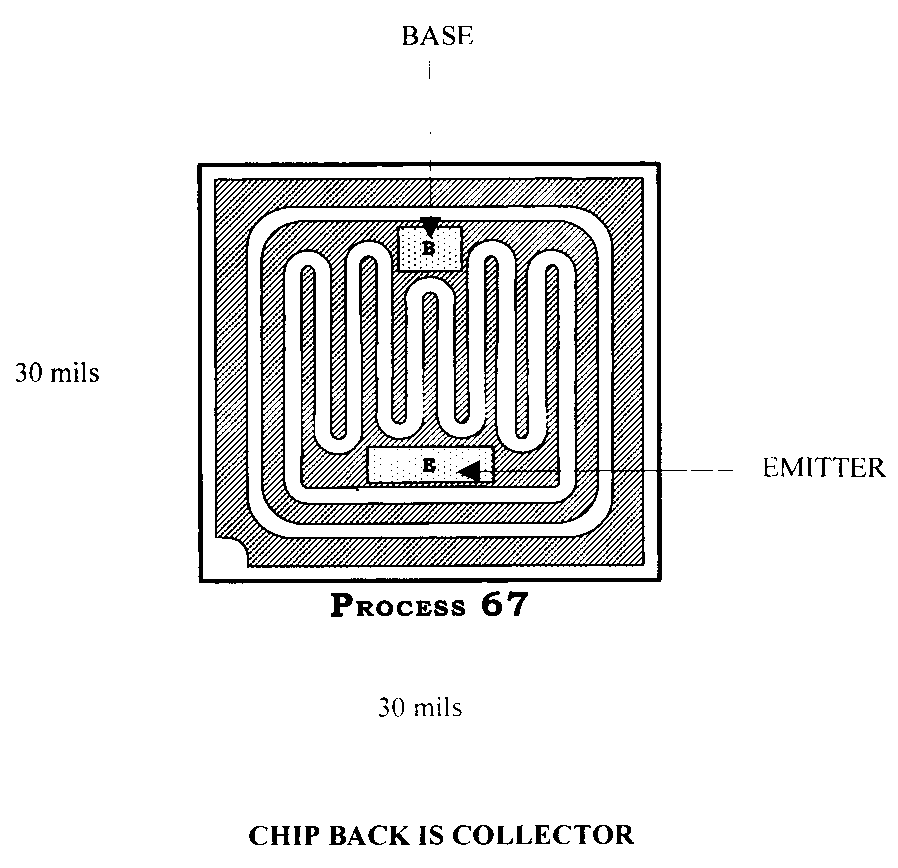
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



**.030”**

**.030”**

**BASE**

**EMITTER**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: E = .0035” X .009” B = .004” X .005”**

**Backside Potential: Collector**

**Process: 67**

**APPROVED BY: DK DIE SIZE .030” X .030” DATE: 10/6/21**

**MFG: FAIRCHILD THICKNESS .010” P/N: 2N4033**

**DG 10.1.2**

#### Rev B, 7/19/02